SPECIFICATION

High Quality
2+1 Horizontal Hot-Swappable
1U Redundant Power Supply

Universal AC Input
1000W ATX12V Output

P/N: T51000ET 1FH (Whole set)
P/N: R5500ET 1FM (Module only)

*** Specification Approval ***

This specification (total 20 pages including cover page) in its entirety is approved by:

Company Name	Print Name	Signature	Date

Specification subject to change without prior notice.

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1. General

This specification describes the electrical characteristics, functional and physical of a 1000W+550W =1000Watts redundant power supply with Active PFC (Power Factor Correction) and hot-swappable capabilities.

2. AC Input Characteristics

2.1 AC Input Voltage, Frequency and Current (Rating: 100V-240Vac, 47-63Hz, 16-8A)

The power supply must operate within all specified limits over the input voltage range in Table 1. Harmonics distortion of up to 10% THD must not cause the power supply to go out of specified limits.

Parameter	Minimum	Rated	Maximum	Max. Current
Voltage (115V)	90 Vac	100-127Vac	132 Vac	16 A
Voltage (230V)	180 Vac	200-240Vac	264Vac	8 A
Frequency	47 Hz	50 / 60 Hz	63 Hz	

Table 1 – AC Input Voltage , Frequency and Current

2.2 AC Inrush Current

AC line inrush current shall not damage any component nor cause the AC line fuse to blow under any DC conditions and with any specified AC line input voltage and frequency. Repetitive On/Off cycling of the AC input voltage shall not damage the power supply.

2.3 Input Power Factor Correction (Active PFC)

The power factor at full load shall be ≥ 0.95 at nominal input voltage.

2.4 Input Current Harmonics

When the power supply is operated in 90-264Vac of Sec. 2.1, the input harmonic current drawn on the power line shall not exceed the limits set by EN61000-3-2 class "D" standards. The power supply shall incorporate universal power input with active power factor correction.

2.5 AC Line Dropout

An AC line dropout of 17mS or less shall not cause any tripping of control signals or protection circuits. If the AC dropout lasts longer than 17mS the power supply should recover and meet all turn on requirements. The power supply shall meet the regulation requirement over all rated AC voltages, frequencies, and output loading conditions. Any dropout of the AC line shall not cause damage to the power supply. An AC line dropout is defined as a drop in AC line to 0VAC at any phase of the AC line for any length of time.

2.6 AC Line Slow Transients

AC line slow transient conditions shall be defined as "sag" and "surge" conditions. Sag conditions (also referred To as "brownout" conditions) will be defined as the AC line voltage dropping below nominal. Surge Conditions will be defined as the AC line voltage rising above nominal voltage.

The power supply shall meet the regulation requirements under the following AC line sag and surge conditions.

Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Input ranges	50/60 Hz	No loss of function or performance
0-1 AC cycle	100%	Nominal AC Input ranges	50/60 Hz	No loss of function or performance
> 1 AC cycle	>10% (110V) >30% (220V)	Nominal AC Input ranges	50/60 Hz	Loss of function Acceptable, self recoverable

Table 3 – AC Line Sag Transient Performance

Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltage	50/60 Hz	No loss of function or performance
0 - ½ AC cycle	30%	Mid-point of Nominal AC Voltage	50/60 Hz	No loss of function or performance

Table 4 – AC Line Surge Transient Performance

2.7 AC Surge Voltages

The power supply shall be tested and be compliant with the requirements of IEC61000-4-5 Level 3 criteria for surge withstand capability, with the following conditions and exceptions. The test equipment and calibrated waveforms shall comply with the requirements of IEC61000-4-5 for open circuit voltage and short circuit current.

- These input transients must not cause any out of regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.
- The power supply must meet surge-withstand test condition under maximum and minimum DC output load conditions.

2.8 Surge Immunity, IEC61000-4-5

The peak value of the unidirectional surge waveform shall be 2KV for common mode and 1KV for differential mode of transient surge injection. No unsafe operation or no user noticeable degradation is allowed under any condition. Automatic or manual recovery is allowed for other conditions.

2.9 Electrical Fast Transient / Burst, IEC61000-4-4

No unsafe operation allowed under any condition. No user noticeable performance degradation up to 1KV is allowed. Automatic or manual recovery is allowed for other conditions.

2.10 Electrical Discharge, IEC61000-4-2

In addition to IEC61000-4-2, the following ESD tests should be conducted. Each surface area of the unit under test should be subjected to twenty (20) successive static discharges, at each of the follow voltages: 2KV, 3KV, 4KV, 5KV, 6KV, 8KV.

All power supply outputs shall continue to operate within the parameters of this specification, without glitches or interruption, while the power is operating as defined and subjected to 2kV through 10kV ESD pulses. The direct ESD event shall not cause any out of regulation conditions such as overshoot or undershoot. The power supply shall withstand these shocks without nuisance trips of the Over-Voltage Protection, Over-Current Protection, or the remote +5VDC, +12VDC shutdown circuitry.

2.11 Radiated Immunity, IEC61000-4-3

Frequency	Electric Field Strength
27 MHz to 500 MHz, un-modulated	3 V/m

3. DC Output Specification

3.1 Output Current / Loading

The following tables define two power and current rating. The power supply shall meet both static and dynamic voltage regulation requirements for minimum load condition.

Output Voltage	+5V	+3.3V	+12V	-12V	+5VSB
Max. Load	50A	45A	65A	1A	2A
Min. Load	3A	1A	1A	0A	0A

Table 5 – Load Range:

Note 1: The +5 & +3.3 Volt total output shall not exceed 320 W.

Note 2: The +5, +3.3 & +12Volt total output shall not exceed 980W.

Note 3: Maximum continues total DC output power shout not exceed 1000W.

Output # Voltage	V1 +5V	V2 +3.3V	V3 +12V	V4 -12V	V5 5VSB
Max. Load	30A	28A	35A	0.8A	2A
Min. Load	3A	1A	1A	0A	0A

Table 6 Load Range of Power Module

Note 1: The +5 & +3.3 Volt total output shall not exceed 200 Watts.

Note 2: The +5, +3.3 & +12Volt total output shall not exceed 530Watts.

3.2 DC Voltage Regulation, Ripple and Noise

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. All outputs are measured with reference to the return remote sense (ReturnS) signal. The +5V, +12V, -12V and +5VSB outputs are measure at the power supply connectors' references to ReturnS. The +5V and +3.3V is measured at its remote sense signal (+5VS+, +3.3VS+) located at the signal connector.

Output Voltage	+5V	+3.3V	+12V	-12V	+5VSB
Load Reg.	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%
Line Reg.	±1%	±1%	±1%	±1%	±1%
Ripple & Noise	50mV	50mV	120mV	120mV	50mV

Table 7 – Regulation, ripple and noise

Ripple and noise shall be measured using the following methods:

a) Measurements made differentially to eliminate common-mode noise
b) Ground lead length of oscilloscope probe shall be ≤ 0.25 inch.
c) Measurements made where the cable connectors attach to the load.
d) Outputs bypassed at the point of measurement with a parallel combination of 10uF tantalum capacitor in parallel with a 0.1uF ceramic capacitors.
e) Oscilloscope bandwidth of 0 Hz to 20MHz.
f) Measurements measured at locations where remote sense wires are connected.
g) Regulation tolerance shall include temperature change, warm up drift and dynamic load

3.3 Dynamic Loading

The output voltages shall remain within the limits specified in Table 7 for the step loading and within the limits specified in Table 9 for the capacitive loading. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty cycle ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δstep load may occur anywhere within the MIN load to the MAX load shown in Table 5.

Output	Δ Step Load Size / Δ Step Load	Load Slew Rate	Capacitive Load
+5V	30%	0.5 A/uS	5600 uF
+3.3V	30%	0.5 A/uS	3300 uF
+12V	50%	0.5 A/uS	3000 uF
+5VSB	30%	0.5 A/uS	100 uF

Table 8 – Transient Load requirements

3.4 Capacitive Loading

The power supply shall be stable and meet all requirements, except dynamic loading requirements, with the following capacitive loading ranges.

Output	MIN	MAX	Units
+5V	400	4,700	uF
+3.3V	250	6,800	uF
+12V	500	11,000	uF
-12V	1	350	uF
+5VSB	20	350	uF

Table 9 – Capacitive Loading Conditions

3.5 Timing Requirements

These are the timing requirements for the power assembly operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70mS. The +5V, +3.3V and +12V output voltages should start to rise at about the same time. All outputs must rise monotonically. The +5V output needs to be greater than the +3.3V output during any point of the voltage rise. The +5V output must never be greater than the +3.3V output by more than 2.25V. Each output voltage shall reach regulation within 50 mS (T_{vout_on}) of each other during turn on of the power supply. Each output voltage shall fall out of regulation within 400 mS (T_{vout_off}) of each other during turn off. Figure 1 and figure 2 show the turn On and turn Off timing requirement. In Figure 2, the timing is shown with both AC and PSON# controlling the On/Off of the power supply.

Item	Description	MIN	MAX	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	70	mS
T_{vout_on}	All main output must be within regulation of each other within this time.		50	mS
T_{vout_off}	All main output must leave regulation within this time		400	mS

Table 9 – Output Voltage Timing

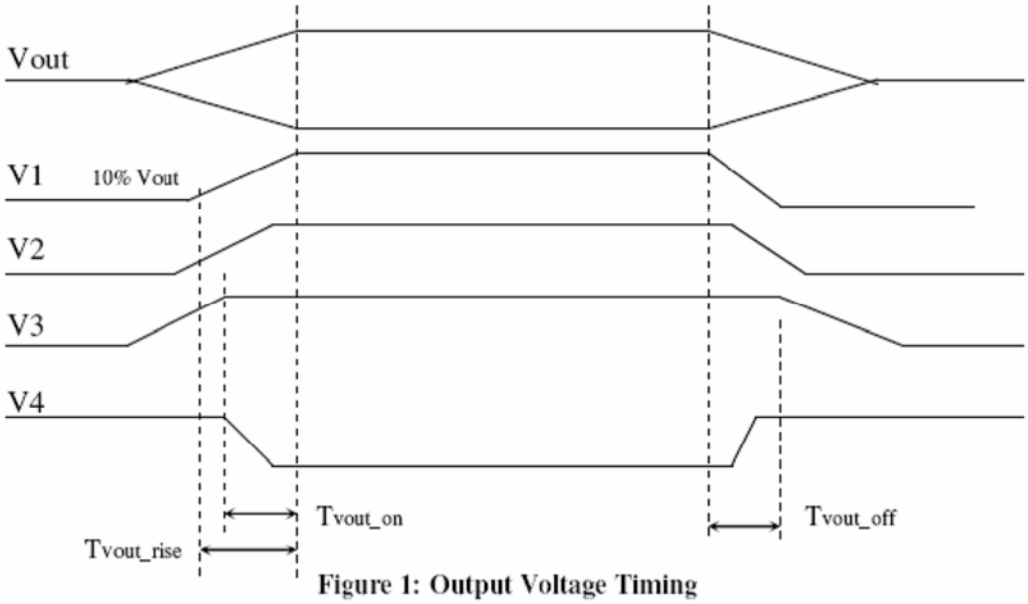


Figure 1: Output Voltage Timing

Item	Description	MIN	MAX	Units
Tsb_on-delay	Delay from AC being applied to +5VSB being within regulation.		1500	mS
Tac_on-delay	Delay from AC being applied to all output voltages being within regulation.		2500	mS
Tvout_holdup	Time all output voltage stay within regulation after loss of AC	17		mS
Tpwok_holdup	Delay from loss of AC deassertion of PWOK.	16		mS
Tpson_on_delay	Delay from PSON# active to output voltage within regulation limits.	5	400	mS
Tpson_pwok	Delay from PSON# deactive to PWOK being deasserted.		50	mS
Tpwok_on	Delay from output voltage within regulation limits to PWOK asserted at turn on.	100	1000	mS
Tpwok_off	Delay from PWOK deasserted to output voltages (+5V, +3.3V, +12V, -12V) dropping out of regulation limits.	1		mS
Tpwok_low	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON# signal. .	100		mS
Tsb_vout	Delay from +5VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	mS

Table 10 – Turn On/Off Timing

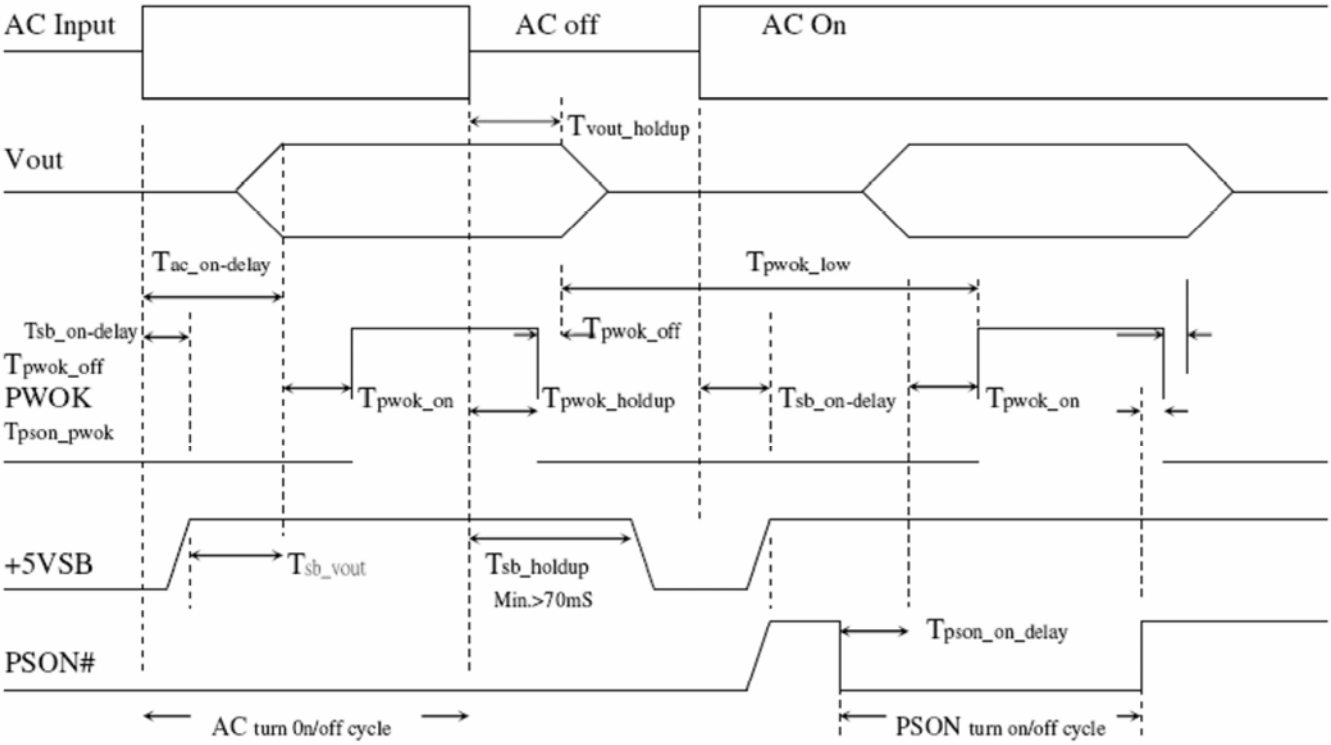


Figure 2: Turn On/Off Timing

3.6 Power Good Signal: PWOK

PSOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be deasserted to a LOW state. See for a representation of the timing characteristics of PWOK. The start of PWOK delay time shall inhibited as long as any power supply output is in current limit.

Signal Type	**Open collector/drain output from power supply. Pull-up to VSB located in power supply.**	
PWOK = High	Power OK	
PWOK = Low	Power is Not OK	
	MIN	MAX
Logic level low voltage, Isink = 4mA	0V	0.4V
Logic level high voltage, Isource = 200 μA	2.0V	5.25V
Sink current, PWOK = Low		4mA
Source current, PWOK = High		2mA
PWOK delay: Tpwok_on	100mSec	1000mSec
PWOK rise and fall time		100 μSec
PWOK down delay: Tpwok_off	2mSec	200mSec

Table 11 – PWOK Signal Characteristics

3.7 Remote On/Off Control: PSON#

The PSON# signal is required to remotely turn on/off the power supply. PSON# is an active low signal that turns on the +5V, +3.3V, +12V and –12V power rails. When this signal is not pulled low by the system, or left open, the outputs (except the +5VSB and Vbias) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply.

Signal Type	**Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.**	
PSON# = Low	Power ON	
PSON# = Open	Power OFF	
	MIN	MAX
Logic level low (Power supply ON)	0V	0.8V
Logic level low (Power supply OFF)	2.4V	5.25V
Source current, Vpson = Low		4mA
Power up delay: $T_{pson\_on\_delay}$	5mSec	400mSec
PWOK delay: T_{pson_pwok}		50mSec

Table 12 – PWOK Signal Characteristics

3.8 Overshoot at Turn-on /Turn-off

Any output overshoot at turn on shall be less than 10% of the nominal output value. Any overshoot shall recover to within regulation in less than 10ms.

3.9 Efficiency

The minimum power supply system efficiency shall be ≥ 65%, measured at nominal input voltage 115 V or 230 V and full loading.

3.10 +5VSB (Standby)

The +5VSB output is always on (+5V Standby) when AC power is applied and power switch is turned on. The +5VSB line is capable of delivering at a maximum of 2.0A for PC board circuit to operate.

4. Protection

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, either a AC cycle OFF for 15 sec, or PSON# cycle HIGH for 1 sec must be able to restart the power supply.

4.1 Over Current Protection

This power supply shall have current limit to prevent the +5V, +3.3V, and +12V outputs from exceeding the values shown in table 13. The current limit shall not trip under maximum continuous load or peak loading as described in Table 5. The power supply shall latch off if the current exceeds the limit. The latch shall be cleared by toggling the PSON# signal or by cycling the AC power. The power supply shall not be damaged from repeated power cycling in this condition. The –12V and +5VSB outputs shall be shorted circuit protected so that no damage can occur to the power supply.

Voltage	Minimum	Maximum	Shutdown Mode
+5V	110%	150%	Latch Off
+3.3V	110%	150%	Latch Off
+12V	110%	150%	Latch Off

Table 13 – Over Current protection

4.2 Over Voltage Protection

The power supply shall shut down in a latch off mode when the output voltage exceeds the over voltage limit shown in Table 4.

Voltage	Minimum	Maximum	Shutdown Mode
+5V	+5.6V	+6.5V	Latch Off
+3.3V	+3.8V	+4.5V	Latch Off
+12V	+13.3V	+15.5V	Latch Off

Table 15 – Over Voltage protection

4.3 Short Circuit Protection

The power supply shall shut down in a latch off mode when the output voltage is short circuit.
Age or hazardous conditions shall occur. In such a case, the power supply shall power up and stabilize.

4.4 No Load Operation

When the primary power is applied, with no load on any output voltage, no damage or hazardous conditions shall occur. In such a case, the power supply shall power up and stabilize.

5. Environmental Requirements

5.1 Temperature

Operating Temperature Range:	0°C ~ 50°C (32°F~ 104°F)
Non-Operating Temperature Range:	-40°C ~ 70°C (-40°F~ 158°F)

5.2 Humidity

Operating Humidity Range:	20% ~ 90%RH non-condensing
Non-Operating Humidity Range:	5% ~ 95%RH non-condensing

5.3 Altitude

Operating Altitude Range:	Sea level to 10,000 ft
Non-Operating Altitude Range:	Sea level to 40,000 ft

5.4 Mechanical Shock

The power supply (non-operating) shall not be damaged during a shock of 50G with an 11mS half sin wave, non-operating. The shock to be applied in each of the orthogonal axes.

5.5 Vibration (Operating and Non-operating)

The power supply shall be subjected to a vibration test consisting of a 10 to 300 Hz sweep at a constant acceleration of 2.0g for duration of one (1) hour for each of the perpendicular axes X, Y and Z,
0.1 octave/minute. The output voltages shall remain within specification.

5.6 Acoustic Noise

The power supply shall be tested in accordance with specifications. The overall sound is measured with the noise meter placed 1 meter from the nearest vertical surface of center of fan installed in power supply.
CONDITIONS LIMITS:
115 VAC Input, full load of +5V Acoustic noise is 50 db maximum, 1A of +12V.

6. Agency Requirements

6.1 Safety Certification.

Product Safety:	UL 60950 2000Edition, IEC60950, 3rd Edition EU Low Voltage Directive(73/23/EEC) (CB) TUV
RFI Emission:	FCC Part15 (Radiated & Conducted Emissions) CISPR 22,3rd Edition/ EN55022 Class B)
PFC Harmonic:	EN 61000-3-2
Flicker:	EN 61000-3-3
Immunity against: **-Electrostatic discharge:** **-Radiated field strength:** **-Fast transients:** **-Surge voltage:** **-RF Conducted** **-Voltage Dips and Interruptions**	EN55024: 1998 -IEC 61000-4-2 Min. 4kV contact discharge Min. 8kV air discharge -IEC 61000-4-3 Min. 10V/m -IEC 61000-4-4 Min 2kV AC input lines Min 1kV on data lines -IEC 61000-4-5 Min 2kV common mode Min 1kV differential mode -IEC 61000-4-6 -IEC 61000-4-11

6.2 Input Leakage Current

Input leakage current from line to ground will be less than 3.5mA rms. Measurement will be made at 240 VAC and 60Hz.

6.3 Production Line Testing

100% of the power supply production must have the following test performed. Each power shall be marked indicating the testing was done and passed. Typically this is done by stamping or labeling the power supply with “Hi-pot test OK”.

6.4 Hi-Pot Testing

Each power supply must be Hi-pot tested according UL and TUV requirements; Minimum typical testing voltage for Hi-pot testing is 1500Vac or 2121Vdc. However depending on the power supply design the testing voltage May be higher. If higher the power supplies shell be at the higher value.

6.5 Ground Continuity Testing

UL and TUV require that each power supply ground is tested, to ensure there is continuity between the ground inlet of the power supply and the power supply chassis. This can be performed with an ohm meter, or an electronic circuit that lights up and illustrates the ground has continuity.

Based on EN50116, ERG or TUV require that each power supply ground id tested with a 25Amp ground test.

Electronic circuit that lights up and illustrates the ground has continuity.

Based on EN50116, ERG or TUV require that each power supply ground id tested with a 25Amp ground test.

7. Redundant Power Supply Function:

7.1 Redundancy

The redundant power supply is N+1=N (1000W+550W=1000W) function power supply, each one module is redundancy when any one module was failed. To be redundant each item must be in the Hot swap power supply module.

7.2 Hot Swap Requirements

The redundant power supply modules shall be hot swappable. Hot swapping a power supply is the process of inserting and extracting a power supply from an operating. During this process the output voltage shall remain within the limits specified in Table 7 with the capacitive load specified Table 9. The Sub-system shall not exceed the maximum inrush current as specified in section 2.2. The power supply can be hot swapped by the following methods:

- AC connecting separately to each module. Up to two power supplies may be on a single AC power source.
  Extraction: The AC power will be disconnected from the power supply first and then the power supply is
  Extracted from the sub-system. This could occur in standby mode or powered on mode. Insertion: The module is inserted into the cage and then AC power will be connected to the power supply module.
- For power modules with AC docking at the same time as DC. Extraction: The module is extracted from thecage and both AC and DC disconnect at the same Time. This could occur in standby or power on mode. No damage or arcing shall occur to the DC or AC contacts which could cause damage. Insertion: The AC and DC connect at the same time as the module is inserted into the cage. No damage to the connector contacts shall occur. The module may power on or come up into standby mode.

Many variations of the above are possible. Supplies need to be compatible with these different variations depending upon the sub-system construction. In general, a failed (off by internal latch or external control) supply may be removed, then replaced with a good power supply(must use the same model) , however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply may get turned on by inserting the supply into the system or by system management recognizing an inserted supply and explicitly turning it on.

7.3 LED Indicators

There shell be a single bi-color LED. The GREEN LED shall turn ON to indicate that all the power outputs are available. The Red LED shall turn ON to indicate that the power supply has failed, shutdown due to over current, or shutdown due to component failure.
The LED(s) shall be visible on the power supply's exterior face. The LED location shall meet ESD requirements. LED shall be securely mounted in such a way that incidental pressure on the LED shall not cause it to become displaced.

-Optional- 8. Field Replacement Unit (FRU)/ I²C Function

8.1 Field Replacement Unit (FRU) Signal

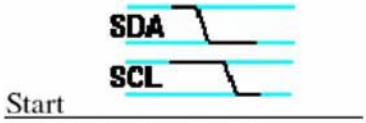
Two pins will be allocated for the FRU information on the power supply connector. One pin is the Serial CLOCK (SCL). The second pin is used for Serial DATA (SDA).

The FRU circuits inside the power supply must be powered off of 5VSB on the system side of the device and grounded to ReturnS (remote sense return). The Write Control (or Write protect) pin should be tied to ReturnS inside the power supply so that information can be written to the EEPROM.

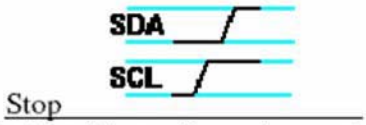
8.2 I²C Bus Events: The START and STOP conditions

Prior to any transaction on the bus, a START condition needs to be issued on the bus. The start condition acts as a signal to all connected IC's that something is about to be transmitted on the bus. As a result, all connected chips will listen to the bus.

After a message has been completed, a STOP condition is sent. This is the signal for all devices on the bus that the bus is available again (idle). If a chip was accessed and has received data during the last transaction, it will now process this information (if not already processed during the reception of the message).



The chip issuing the Start condition first pulls the SDA (data) line low, and next pulls the SCL (clock) line low.



The Bus Master first releases the SCL and then the SDA line.

8.3 SMBus protocols

Each message transaction on SMBus follows the format of one of the defined SMBus protocols. The SMBus protocols are a subset of the data transfer formats defined in the I²C specifications. I²C devices that can be accessed through one of the SMBus protocols are compatible with the SMBus specifications. I²Cdevices that do not adhere to these protocols cannot be accessed by standard methods as defined in the SMBus and ACPI specifications.

8.4 Transferring Data: Byte Format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave can't receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

In some cases, it's permitted to use a different format from the I²C-bus format (for CBUS compatible devices for example). A message, which starts with such an address, can be terminated by generation of a STOP condition, even during the transmission of a byte. In this case, no acknowledge is generated.

8.5 Transferring Data: Acknowledge

Data transfer with acknowledges is obligatory. The master generates the acknowledge-related clock pulse. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.

The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. Of course, set-up and hold times must also be taken into account.
Usually, a receiver, which has been addressed, is obliged to generate an acknowledge after each byte has been received, except when the message starts with a CBUS address

When a slave doesn't acknowledge the slave address (for example, it's unable to receive or transmit because it's performing some real-time function) the data line that must be left HIGH by the slave. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.
If a slave-receiver does acknowledge the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer.

The slave generating the not-acknowledge on the first byte to follow indicates this. The slave leaves the data line HIGH and the master generates a STOP or a repeated START condition.

If a master-receiver is involved in a transfer, it must signal the end of data to the slave- transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a STOP or repeated START condition

Full rated load
120V AC input
Ground Benign
25℃

9. Connections

9.1 AC Input Connector

The AC input receptacle shall be an IEC 320 type or equivalent. The IEC 320 C receptacle will be considered the mains disconnect.

9.2 DC Wire Harness and Connector Requirements

P1: ATX Motherboard Power Connector

Connector housing: 24- Pin Molex 5557 (No.39-01-2240) or Equivalent

Contact: Molex 5556T (No.44476-1111) or Equivalent

Pin	Signal	Color	Size	Pin	Signal	Color	Size
1	+3.3 VDC	Orange	16 AWG	13	+3.3 VDC +3.3VRS+	Orange Brown	16 AWG 22AWG
2	+3.3 VDC	Orange	16 AWG	14	-12 VDC	Blue	18 AWG
3	COM	Black	18 AWG	15	COM	Black	18 AWG
4	+5 VDC	Red	18 AWG	16	PS_ON#	Green	22 AWG
5	COM	Black	18 AWG	17	COM	Black	18 AWG
6	+5 VDC	Red	18 AWG	18	COM	Black	18 AWG
7	COM	Black	18 AWG	19	COM	Black	18 AWG
8	PW_OK	Gray	22 AWG	20	N/C	--	--
9	5VSB	Purple	18 AWG	21	+5 VDC	Red	18 AWG
10	+12 V3DC	Yellow	18 AWG	22	+5 VDC +5V RS+	Red Red	18 AWG 22AWG
11	+12 V3DC	Yellow	18 AWG	23	+5 VDC	Red	18 AWG
12	+3.3 VDC	Orange	16 AWG	24	COM	Black	18 AWG

P2: Processor Power Connector

Connector housing: 8- Pin Molex 5557 (39-01-2080) or Equivalent

Contact: Molex 5556T (44476-1111) or Equivalent

Pin	Signal	Color	Size	Pin	Signal	Color	Size
1	COM	Black	18 AWG	5	+12 V1DC	Yellow	18 AWG
2	COM	Black	18 AWG	6	+12 V1DC	Yellow	18 AWG
3	COM	Black	18 AWG	7	+12 V2DC	Yellow	18 AWG
4	COM	Black	18 AWG	8	+12 V2DC	Yellow	18 AWG

4-Pin HDD / CD-ROM Drive Power Connectors

Connector housing: 4- Pin AMP: 1-480424-0 or Molex 8981-04P or Equivalent

Contact: Amp 61314-1 or Equivalent

Pin	Signal	Color	Size
1	+12 V3DC	Yellow	18 AWG
2	COM	Black	18 AWG
3	COM	Black	18 AWG
4	+5 VDC	Red	18 AWG

Small 4-Pin: Floppy Disk Drive Power Connectors

Connector housing: 4- Pin AMP: 171822-4 or Equivalent

Pin	Signal	Color	Size
1	+5 VDC	Red	22 AWG
2	COM	Black	22 AWG
3	COM	Black	22 AWG
4	+12 V3DC	Yellow	22 AWG

10. Physical Characteristics Size

10.1 Weight: 6.0Kg

10.2 Dimension: 313.6mm(W) x 41.2mm(H) x 325mm(D)

11. Drawing